B2 Cont'd

the substrate, the surface strap providing a connection between the capacitor and the transfer device.

Remarks

In the office action, the Examiner require restriction to one of three groups. Applicants had previously elected group I, with group I including claims 1-29. Applicants have above canceled claims 30-45 and thus have affirmed this election. Applicants also note that the Office Action Summary sheet provided erroneously stated that claims 18-45 where withdrawn from consideration, when in fact only claims 30-45 where withdrawn. Applicants note that the Examiner did in fact consider all of the claims 1-29 in the office action.

In the office action, the Examiner stated that the application has been filed with informal drawings, and that formal drawings incorporating the changes listed in the enclosed PTO-948 will be required. Applicants respectfully submit that the drawings submitted were in fact formal. Furthermore, applicants note that the PTO-948 form states that the draftsperson does not object to the drawings. Thus, applicants submit that the Examiner's request for new drawings is incorrect, and that the drawings on file are sufficient.

Claim 1 was rejected by the Examiner under 35 U.S.C. § 102(b) as being anticipated by Esch, et al. (U.S. Patent No. 4,240,845, hereinafter "Esch").

With respect to claim 1, the Examiner stated that Esch describes a method for forming interconnect between a storage capacitor (citing FIG. 3F, #45, col. 15, line 44-45) and transfer device (citing FIG. 3M, metal word line) in a memory cell including: Forming a capacitor having a lip extending over the top (FIG. 3, F-I, #49, col. 15, lines 50-52) and diffusing dopant from the lip into the top surface of the substrate (FIG. 3G, col. 15, lines 53-64).

In response, applicants submit that the amended claim 1 is patentably distinct over the cited references. First, applicants note that the claim 1 is directed toward a method for forming "an interconnection between a storage capacitor and a transfer device in a memory cell". Second, applicants note that the method of claim 1 recites:

> a) forming a capacitor having a **lip** extending over **a top surface** of a substrate; and
>
> b) diffusing dopant **from the lip** into the top surface of the substrate, the diffusing dopant forming a **surface strap** in the substrate, the surface strap providing a connection between the capacitor and the transfer device.

Thus, the amended claim recites the formation of a **surface strap** connection between a storage capacitor and transfer device by diffusing dopant **from the lip** of the capacitor and **into the top surface** of the substrate. Applicants can find no such process in the cited reference. In the office action, the Examiner cited element 49 in FIGS. 3F to 3I as comprising the lip. Furthermore, the Examiner stated that the diffusing of dopants from the lip and into the top surface of the substrate is disclosed in FIG. 3G and column 15, lines 53-64. Applicants respectfully disagree and note that the cited portion of column 15 (lines 53-64) describe the doping of element 49, and element 49 was cited by the Examiner as including the claimed "lip". Thus, this process puts dopants **into** element 49. However, nowhere in these cited portions is dopant diffused "**from the lip**" into the "top surface" to form a "surface strap", as claimed by the applicants.

This interpretation of the cited Esch reference is further supported by the fact that other node of the capacitor in Esch, element 41, is already directly connected to the transfer device (where the transfer device comprises the FET made with gate dielectric 52, and source/drain regions 44 and 45 (see FIG. 3G). Finally, the portions of element 49 that extend over the substrate are separated from the substrate by silicon dioxide layer 41, presumably preventing dopants from diffusing into the substrate 39 to form a surface strap.

Thus, applicants submit that claim 1 is patentably distinct over the cited Esch reference. Furthermore, as claims 2-17 depend from, and include all the limitations of amended claim 1, thy are also submitted to be patentably distinct.

Claims 2-29 were rejected by the Examiner under 35 U.S.C. § 103(a) as being unpatentable over Esch as applied to claim 1, and further in view of Saenger, et al. (U.S. Patent No. 5,633,781, hereinafter "Saenger") .

With respect to claims 2 and 3, the Examiner stated that Esch describes a method for forming interconnect between a storage capacitor (again citing FIG. 3F, #45, col. 15, lines 44-45) and transfer device (metal line) (again citing FIG. 3M, metal word line) in a memory cell including: Forming a first layer (FIG. 3A, #41, col. 15, line 14) on the substrate (FIG. 3A, #39, col. 15, line 13-14), etching a capacitor opening (FIG. 3E, #47, col 15, lines 39-42). The Examiner then admitted that Esch does not specifically disclose the information of sidewall spacers, but stated that Saenger discloses a sidewall spacer in FIG. 1, #18, col. 3, lines 49-50 to isolate the electrode with a high dielectric constant material. The Examiner then concluded that it would have been obvious to one of ordinary skill in the art at the time of the invention to include Saenger's sidewall spacers in Esch's process to isolate the electrode with a high dielectric constant material. (Citing Saenger col. 4, lines 55-65). The Examiner stated that etching a trench in the substrate (Esch FIG. 3C, #44, 45, col. 15, line28), removing sidewall spacer (Esch FIG. 3 H) filing the trench with polysilicon capacitor fill material (Esch FIGS. 3 E-m, col. 15 lines 42-60).

Again, applicants respectfully disagree. Applicants again note that Esch does not teach formation of a **surface strap** connection between a storage capacitor and transfer device by diffusing dopant **from the lip** of the capacitor and **into the top surface** of the substrate, as discussed above with respect to claim 1. Furthermore, while applicants admit that there are similar steps, when examined individually, between the process cited in claim 2 and those disclosed by Esch, the similar steps in Esch are not used in anything close to the method

recited in claim 2. For example, the steps of claim 2 clearly form a capacitor having a lip extending over the top surface of the substrate, where that lip is used to form a surface strap to connect the capacitor to a transfer device. The formation of the sidewall spacer in oversized capacitor openings is an integral part of this claimed method. Nothing in the cited reference comes close to the process. Instead, the steps recited from Esch are seemingly unrelated with the formation of the sidewall spacer in Saenger.

Furthermore, applicants note that the Examiner gave no explanation as to how the sidewall spacers of Saenger could be incorporated into the process of Esch, and how this would result in the formation of a "capacitor having a lip extending over the top surface of the substrate" where that lip is then used to form a surface strap. Without such an Explanation, applicants submit it is improper to combine the two references. Thus, applicants submit that 2 is patentably distinct over the cited references.

With respect to claim 5, the Examiner stated that Esch describes diffusing done by annealing (Esch col. 16, line 30). Applicants note again that this annealing in Esch does not result in the diffusion of dopants from a lip of a capacitor and into the top surface to connect the capacitor to a transfer device, as claimed by the applicant.

With respect to claims 10-11, the Examiner essentially repeated the arguments for the above claims. Applicants respectfully disagree for the reasons given above. Specifically, the applicants again note the recited method forms a capacitor having a lip, with a process that uses oversized capacitor openings and sidewall spacers (where the lip is then used to form a surface strap). Applicants cannot find any similar process in the cited reference.

With respect to claims 12-15, the Examiner stated that Esch describes a method for forming interconnect between a storage capacitor (FIG. 3F, #45, col. 15, lines 44-45) and transfer device (metal line) (FIG. 3M, metal word line) in a memory cell including:

The Examiner stated that claims 12 and 15 repeat all the steps of claims 1-11 and adds the step of source/drain implants (Esch col. 16, lines 29-35), patterning the word line by etching (Esch FIG. 4, 4M, col. 16, lines 46-56) removing a portion of insulator (Esch FIG. 3H). Applicants disagree, and note that the claimed steps of forming source/drain, wherein the **dopant diffused from the lip to the top surface comprises a source/drain** of the transfer device. Nothing comparable is seen in the cited references.

The remainder of the rejections given by the Examiner essentially restate the rejections discussed above. Thus, for the same reasons applicants submit that claims 17-29 are patentably distinct. Again, applicants note that none of the cited references disclose the formation of a **surface strap** connection between a storage capacitor and transfer device by diffusing dopant **from the lip** of the capacitor and **into the top surface** of the substrate. Furthermore, none of the cited references discloses the formation of oversized capacitor openings and the use of sidewall spacers to form the capacitor lip, as claimed.

It is therefore submitted that the application, as presently amended, defines patentable subject matter. Therefore, applicants' claims currently on file are in condition for allowance. Such allowance at an early date is respectfully requested.

Applicants hereby declare that any amendments herein that are not specifically made for the purpose of patentability are made for other purposes, such as clarification, and that no such changes shall be construed as limiting the scope of the claims or the application of the Doctrine of Equivalents.

Docket No. BU9-97-149

If any fees, including extension of time fees, are due as a result of this response, please charge IBM Corp Deposit Account No. 09-0456 authorization is intended to act as a constructive petition for an extension of time, should an extension of time be needed as a result of this response. The examiner is invited to telephone the undersigned if this would in any way advance the prosecution of this case.

Respectfully submitted,

By _____
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VERSION OF ALL CLAIMS WITH MARKINGS TO SHOW CHANGES MADE

Claim 1. (Amended) A method for forming an interconnection between a storage capacitor and a transfer device in a memory cell, the method comprising the steps of:

a) forming a capacitor having a lip extending over a top surface of a substrate; and

b) diffusing dopant from the lip into the top surface of the substrate, the diffusing dopant forming a surface strap in the substrate, the diffusing dopant forming a surface strap in the substrate, the surface strap providing a connection between the capacitor and the transfer device.

Claim 2. (Unchanged) The method of claim 1 wherein the step of forming a capacitor having a lip extending over a top surface of a substrate comprises:

i) forming a first layer on the substrate;

ii) etching an oversized capacitor opening in the first layer;

iii) forming a sidewall spacer on sidewall of the oversized capacitor opening;

iv) etching a trench in the substrate using the sidewall spacer as a mask;

v) removing the sidewall spacer; and

vi) filling the trench and oversized capacitor opening with capacitor fill material.

Claim 3. (Unchanged) The method of claim 2 wherein the capacitor fill material comprises polysilicon.

Claim 4. (Unchanged) The method of claim 2 wherein the step of forming a capacitor having a lip extending over a top surface of a substrate further comprises:

vii) recessing the capacitor fill material partially into the oversized capacitor opening; and

viii) filling the recess in the oversized capacitor opening with a dielectric material.

Claim 5. (Unchanged) The method of claim 1 wherein the step of diffusing dopant from the lip into the top surface comprises annealing the substrate and the capacitor.

Claim6. (Unchanged) The method of claim 1 wherein the first layer comprises a gate stack including:

i) a gate dielectric layer;

ii) a gate conductor layer on the gate dielectric layer; and

iii) an insulator layer on the gate conductor layer.

Claim 7. (Unchanged) The method of claim 6 wherein the gate conductor layer comprises polysilicon.

Claim 8. (Unchanged) The method of claim 6 wherein the insulator layer comprises a layer of silicon nitride and a layer of silicon dioxide.

Claim 9. (Unchanged) The method of claim 1 wherein the first layer comprises a layer of silicon dioxide, a layer of silicon nitride, and an a layer of silicon dioxide.

Claim 10. (Unchanged) The method of claim 1 wherein the step of forming a capacitor comprises the steps of:

i) forming a gate stack, the gate stack including a gate dielectric, a gate conductor on the gate dielectric, and an insulator layer on the gate conductor;

ii) etching an oversized capacitor opening in the gate stack;

iii) forming a sidewall spacer on sidewall of the oversized capacitor opening;

iv) etching a trench in the substrate using the sidewall spacer and the insulator layer on the gate conductor as a mask;

v) removing the sidewall spacer;

vi) forming an oxide collar in the trench;

vii) filling the trench and oversized capacitor opening with a capacitor fill material thereby forming a lip of capacitor fill material at the top of the trench;

viii) recessing the capacitor fill material partially into the oversized capacitor opening;

ix) filling the recess in the oversized capacitor opening with a dielectric material; and

x) forming shallow trench isolation, the shallow trench isolation removing portions of the lip except where a connection from the capacitor to the transfer device is to be formed.

Claim 11. (Unchanged) The method of claim 10 further comprising the steps of:

d) patterning the remaining gate conductor stack; and

e) forming sidewall spacers on the sidewalls of the patterned gate conductor stack.

Claim 12. (Unchanged) The method of claim 1 wherein the step of forming a capacitor comprises the steps of:

i) forming a gate stack, the gate stack including a gate dielectric, a gate conductor on the gate dielectric, and an insulator layer on the gate conductor;

ii) etching an oversized capacitor opening in the gate stack;

iii) forming a sidewall spacer on sidewall of the oversized capacitor opening;

iv) etching a trench in the substrate using the sidewall spacer and the insulator layer on the gate conductor as a mask;

v) removing the sidewall spacer;

vi) forming an oxide collar in the trench;

vii) filling the trench and oversized capacitor opening with a capacitor fill material thereby forming a lip of capacitor fill material at the top of the trench;

viii) recessing the capacitor fill material partially into the oversized capacitor opening;

ix) filling the recess in the oversized capacitor opening with a dielectric material;

x) forming shallow trench isolation, the shallow trench isolation removing portions of the gate stack and portions of the capacitor lip except where a connection from the capacitor to the transfer device is to be formed;

xi) planarizing shallow trench isolation and the remaining gate stack, such that a portion of the insulator layer remains on the gate conductor layer;

xii) removing a portion of the remaining insulator layer between shallow trench isolation regions, the removal exposing portions of the underlying gate conductor material;

xiii) depositing wordline line material that contacts the exposed gate conductor material;

Claim 12 Continued:

xiv) patterning the wordline and gate conductor material to form a plurality of gates;

xv) forming a source/drain implants; and

wherein the step of diffusing dopant from the lip into the top surface of the substrate comprises annealing, and wherein the dopant diffused from the lip to the top surface comprises a source/drain of the transfer device and wherein the source/drain implant diffuses to form a source/drain of the transfer device.

Claim 13. (Unchanged) The method of claim 12 wherein the step of patterning the wordline and gate conductor material comprises etching selective to the remaining insulator material to avoid etching the gate conductor material at portions adjacent to the capacitor.

Claim 14. (Unchanged) The method of claim 12 wherein the step of removing a portion of the remaining insulator layer between shallow trench isolation regions comprises leaving a portion extending into area where the gate will be formed to compensate for potential alignment errors.

Claim 15. (Unchanged) The method of claim 1 wherein the step of forming a capacitor comprises the steps of:

i) forming a first layer on the substrate, the first layer comprising a first silicon dioxide layer, a silicon nitride layer and second silicon dioxide layer;

ii) etching an oversized capacitor opening in the first layer;

iii) forming a sidewall spacer on sidewall of the oversized capacitor opening;

iv) etching a trench in the substrate using the sidewall spacer and the first layer as a mask;

v) removing the sidewall spacer;

vi) forming an oxide collar in the trench;

vii) filling the trench and oversized capacitor opening with a capacitor fill material thereby forming a lip of capacitor fill material at the top of the trench;

viii) recessing the capacitor fill material partially into the oversized capacitor opening;

ix) filling the recess in the oversized capacitor opening with a dielectric material;

x) forming shallow trench isolation, the shallow trench isolation removing portions of the lip except where a connection from the capacitor to the transfer device is to be formed.

Claim 16. (Unchanged) The method of claim 12 further comprising the steps of:

c) removing remaining portions of the first layer;

d) forming gate dielectric;

e) depositing a gate conductor material;

f) patterning the gate conductor.

Claim 17. (Unchanged) A method for forming a connection between a capacitor and a transfer device on a semiconductor substrate having a top surface, the method comprising the steps of:

a) forming a first layer on the semiconductor substrate;

b) etching an oversized capacitor opening in the first layer;

c) forming a sidewall spacer on the sidewalls of the oversized capacitor opening;

d) etching a capacitor trench in the semiconductor substrate using said sidewall spacer and said first layer as a mask, said capacitor trench having a top edge at the top surface of said semiconductor substrate;

e) depositing capacitor fill material in said capacitor trench, said capacitor fill material extending over said capacitor trench top edge to form a lip of capacitor fill material on said top surface of said semiconductor substrate; and

f) diffusing dopants from said capacitor fill material into said semiconductor substrate from said lip of capacitor fill material, the diffusing dopant forming a surface strap in the substrate, the surface strap providing a connection between the capacitor and the transfer device.

Claim 18. (Unchanged) The method of claim 17 wherein the first layer comprises a gate dielectric layer, a gate conductor layer and a insulator layer.

Claim 19. (Unchanged) The method of claim 17 wherein the first layer comprises a first silicon dioxide layer, a silicon nitride layer and second silicon dioxide layer.

Claim 20. (Unchanged) The method of claim 17 wherein the step of depositing capacitor fill material comprises performing a first deposition of capacitor fill material, recessing said first deposition of capacitor fill material, said recess partially exposing sidewalls of said capacitor trench, forming sidewall spacers on said exposed sidewalls of said capacitor trench, and refilling the capacitor trench and oversized capacitor opening.

Claim 21.(Unchanged) The method of claim 17 wherein the capacitor fill material comprises n+ doped polysilicon.

Claim 22. (Unchanged) The method of claim 17 wherein the step of diffusing dopants from said capacitor fill material into said semiconductor substrate from said lip of capacitor fill material comprises annealing the semiconductor substrate.

Claim 23. (Unchanged) The method of claim 17 further comprising the step of etching an isolation trench, wherein said etching of said isolation trench removes a portion on said lip of capacitor fill material except where a connection between said capacitor and said transfer device is to be made.

Claim 24. (Unchanged) The method of claim 23 further comprising the step of filling said isolation trench with isolation material and planarizing said isolation material.

Claim 25. (Unchanged) The method of claim 24 wherein the first layer comprises a gate dielectric layer, a gate conductor layer and a insulator layer and wherein the step of planarizing said isolation material removes said insulator layer to expose said gate conductor material.

Claim 26. (Unchanged) The method of claim 24 wherein the first layer comprises a gate dielectric layer, a gate conductor layer and a insulator layer and wherein the step of planarizing said isolation material leaves a portion of the insulator layer covering the gate conductor layer.

Claim 27. (Unchanged) The method of claim 25 further comprising the step of depositing a wordline material layer on said gate conductor material and said isolation material, and further comprising the step of patterning the gate conductor material and wordline material to form a plurality of transfer device gates.

Claim 28. (Unchanged) The method of claim 26 further comprising the steps of etching an opening in the remaining portion of the insulator layer to expose a portion of the gate conductor layer and depositing a wordline material layer on the exposed gate conductor material, the remaining insulator layer and the isolation material, and further comprising the step of patterning the gate conductor material and wordline material to form a plurality of transfer device gates, wherein the remaining insulator layer serves as an etch block to prevent unwanted etching of the gate conductor material.

Claim 29. (Unchanged) The method of claim 24 wherein the first layer comprises a first silicon dioxide layer, a silicon nitride layer and second silicon dioxide layer wherein the step of planarizing said isolation material removes any remaining portion of said second silicon dioxide layer and planarizes said silicon nitride layer, and further comprising the step of removing said silicon nitride layer and forming a gate dielectric layer, a gate conductor layer, and a wordline material layer, and further comprising the step of pattering said gate dielectric layer, said gate conductor layer and said wordline material layer to define a gate of the transfer device.

Claim 30. (Canceled)

Claim 31. (Canceled)

Claim 32. (Canceled)

Claim 33. (Canceled)

Claim 34. (Canceled)

Claim 35. (Canceled)

Claim 36. (Canceled)

Claim 37. (Canceled)

Claim 38. (Canceled)

Claim 39. (Canceled)

Claim 40. (Canceled)

Claim 41. (Canceled)

Claim 42. (Canceled)

Claim 43. (Canceled)

Claim 44. (Canceled)

Claim 45. (Canceled)